REMARKS

The present application includes pending claims 1-33, all of which remain rejected. The Applicants respectfully submit that the claims define patentable subject matter.

Claims 1-5, and 7-33 remain rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,757,746 ("Boucher"). Claim 6 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher. The Applicants respectfully traverse these rejections at least for the following reasons:

I. Boucher Does Not Anticipate Claims 1-5, And 7-33

The Applicants first turn to the rejection of claims 1-5, and 7-33 as being anticipated by Boucher.

A. Boucher Does Not Teach Or Suggest "Processing Occurring Without Reassembly"

The Office Action responds to the Applicants' previous remarks regarding Boucher not teaching or suggesting "processing occurring without reassembly" as follows:

> Applicant is utilizing the term "reassembly" in the claim for reassembling TCP/IP packets which were fragmented (see specification, page 11, ¶ 39).

See October 7, 2005 Office Action at page 6.

Claim 1, for example, recites, in part, the following:

> at least one internal elastic buffer, wherein **said TEEC processes an incoming TCP packet** once and temporarily buffers at least a portion of said incoming

> TCP packet in said internal elastic buffer, **said processing occurring without reassembly**.

See claim 1 (emphasis added). Thus, the relevant processing is that which is performed by the TEEC with respect to an incoming TCP packet. This processing which is performed by the TEEC with respect to an incoming TCP packet occurs without reassembly.

The Office Action seemingly imports portions of the specification into the claims. *See* October 7, 2005 Office Action at page 5 ("Applicant is utilizing the term in the claim for reassembling TCP/IP packets which were fragmented (see specification, page 11, ¶ 39)"). The Applicants are perplexed that the Office Action imports language from the specification into the claims, because such a practice runs afoul of patent examining procedure. *See, e.g.,* Manual of Patent Examining Procedure at § 2111.01(I) ("One must bear in mind that, especially in nonchemical cases, the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification."). "Though understanding the claim language may be aided by explanations contained in the written description, **it is important not to import into a claim limitations that are not part of the claim**." *See id.* (emphasis added, internal citation omitted). The language of claim 1 is clear and should stand on its own, without limitations from the specification being read into it.

The Office Action further states the following:

> The memory used in the ASIC is not for this purpose [i.e., reassembly], rather this is done in the host memory as can be seen in '173, Figures 23 and Figure 2, of Boucher.

See October 7, 2005 Office Action at page 6. The Applicants respectfully disagree.

The Office Action cites "ASIC 400 disclosed in Figure 21 of app. No. 09/464,283, USPN 6,427,173 incorporated by reference" as a TEEC. *See* August 19, 2005 Office Action at pages 3-4. Boucher states that in "one specific embodiment, NI device 102 is the Intelligent Network Interface Card (NIC) of FIGS. 21 and 22 of U.S. patent application Ser. No. 09/464,283 [United States Patent No. 6,427,173 ("Boucher '173")] (the entire disclosure of Ser. No. 09/464,283 is incorporated... by reference). *See* Boucher at column 1, lines 22-25. Boucher '173 states that "INIC card 200 includes a Physical Layer Interface (PHY) chip 2100, ASIC chip 400 and Dynamic Random Access Memory (DRAM) 460." *See* Boucher '173 at column 24, lines 60-63. As noted above, the DRAM 460 is separate and distinct from the ASIC chip 400.

The ASIC chip 400 includes a sequencers block 2102 that includes a data synchronization buffer and a data assembly register.

> ASIC chip 400 includes a Media Access Control (MAC) unit 402, a sequencers block 2102, SRAM control 442, SRAM 440, DRAM control 450, a queue manager 2103, a processor 470, and a PCI bus interface unit 468.... Sequencers block 2102 includes a transmit sequencer 2104, **a receive sequencer 2105**, and configuration registers 2106.

Id. at column 24, line 67 to column 25, line 13. As shown above, the receive sequencer 2105 is part of the sequencers block 2102, which is, in turn, part of the ASIC chip 400. Therefore, the ASIC chip 400 includes the receive sequencer 2105.

The receiver sequencer 2105 does, in fact, include much more than mere memory, as suggested by the Office Action ("The memory used in the ASIC is not for this purpose..."). As shown below, the receiver sequencer 2105, which is part of the ASIC chip, includes a data assembly register.

> FIG. 22 is a more detailed diagram of receive sequencer 2105. Receive sequencer 2105 includes a data synchronization buffer 2200, a packet synchronization sequencer 2201, a **data assembly register 2202**, ...

Id. at column 25, lines 17-21 (emphasis added). Clearly, the data assembly register 2202 is used to assemble data at the receive sequencer 2105, which is part of the ASIC chip 400. Data is assembled within the ASIC chip 400 (which the Office Action assumes is a TEEC), by way of at least the data assembly register 2202. Thus, Boucher does not teach or suggest "processing occurring [by a TEEC] **without reassembly**," as recited in the claims of the present application, because reassembly is occurring at the ASIC chip 400 by way of the data assembly register 2202. At least for this reason, the Applicants respectfully submit that Boucher does not anticipate the claims of the present application.

B. Boucher Does Not Teach Or Suggest "A TEEC Including At Least One Internal Elastic Buffer, Wherein The TEEC Processes An Incoming TCP Packet Once And Temporarily Buffers At Least A Portion Of Said Incoming TCP Packet In Said Internal Elastic Buffer"

In response to the Applicants' previous remarks regarding Boucher not teaching or suggesting a TEEC including at least one internal elastic buffer, wherein the TEEC processes an incoming TCP packet once and temporarily

buffers at least a portion of said incoming TCP packet in said internal elastic buffer, the Office Action states the following:

> Applicant will see that data synchronization buffer 2200 is a buffer on the ASIC chip (by virtue of being in the receive sequencer) and is not a multi megabyte memory that is utilized for packet reordering, reassembly or retransmission (it is merely there to store the packet as it is clocked into the receive sequencer). By this rationale, the data synchronization buffer is equivalent to the claimed internal elastic buffer.

See October 7, 2005 Office Action at page 6. The Applicants respectfully submit, however, that the synchronization buffer 2200 is not "merely there to store the packet as it is clocked into the receive sequencer," as shown below.

While Boucher '173 states that the receive sequencer 2105 includes a "data synchronization buffer 2200" (*See id.* at column 25, lines 19-20), Boucher also states the following:

> Receiver sequencer 2105 uses **the buffers in DRAM 460 to store incoming network packet data** as well as status information for the packet.

Id. at column 26, lines 3-5 (emphasis added). Thus, Boucher clearly states that the DRAM 460, not the data synchronization buffer 2200, stores incoming network packet data.

As noted above, DRAM 460 is separate and distinct from the ASIC 400. The ASIC 400, however, does not include at least one internal elastic buffer, wherein the ASIC processes an incoming TCP packet once and temporarily buffers at least a portion of the incoming TCP packet in the internal elastic buffer. Instead, the receive sequencer 2105 uses the buffers in DRAM 460 to

store incoming network packet data, as noted above. Further, the ASIC chip 400 of Boucher, which the Office Action assumes is the TEEC, does not "process an incoming TCP packet once and temporarily buffers at least a portion of the incoming TCP packet" in the data synchronization buffer 2200, which the Office Action assumes is the internal elastic buffer. Boucher does not teach, nor suggest, a TEEC including at least one internal elastic buffer, wherein the TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, as recited, for example, in claim 1 of the present application. Thus, at least for this reason, the Applicants respectfully submit that Boucher does not anticipate the claims of the present application.

II. Inherency

With respect to claim 9, the previous Office Action asserted that "it is inherent that any packet received would be inserted in its correct placement in host memory as shown by Figure 2." *See* August 19, 2005 Office Action at page 5. The Applicants previously submitted that absent a "basis in fact and/or technical reasoning" for the rejection of record, that rejection should be reconsidered and withdrawn. *See* September 15, 2005 Amendment at pages 14-16. In response, the present Office Action states the following:

> Applicant is invited to look at Figure 2 of Boucher, where it is shown that subsequent data packets are received onto the NI device, which have headers stripped, and then the data is DMA'd directly over to the host memory, no reassembly is done in the NIC device, the reassembly is done at the host memory. By this rationale, the rejection is maintained.

See October 7, 2005 Office Action at page 6.

Initially, the Applicants respectfully submit that the ASIC 400 of Boucher performs reassembly, as shown and detailed above. Also, claim 9 recites, in part, "said NIC does not require a dedicated memory for assembling and re-ordering IP packets fragmented at the IP layer." The previous Office Action affirmatively recited that "it is inherent that **any packet** received would be inserted in its **correct placement** in host memory as shown by Figure 2."

The Applicants respectfully disagree with this statement of inherency. For example, when a packet is received in error it must be retransmitted. As a result, packets are often received out-of-order. If the out-of-order packets are to be assembled by the NIC and sent up to the host, a larger ON-NIC memory is required to store and reassemble the out-of-order packets. After the packets are reassembled on the NIC, the packets are posted in the host buffer, and the host is informed that the buffer is posted. The Applicants note that claim 1, for example, recites an "elastic buffer," not a dedicated ON-NIC memory. The Applicants respectfully maintain that it is **not** inherent that any packet received would be inserted in its correct placement in the host memory.

The Applicants once again reviewed and analyzed Figure 2 of Boucher, and maintain that there is nothing in that Figure to lead one to conclude that any packet that is received would **necessarily** be inserted in its correct placement in host memory, as asserted by the Office Action.

Additionally, claim 9 recites that that the "NIC," not the host, "does not require a dedicated memory for assembling and reordering IP packets

fragmented at the IP layer." The Office Action, however, concludes that Figure 2 shows placement in the host memory.

The Applicants submit that a rejection based on inherency **must** include a statement of the rationale or evidence tending to show inherency. *See* Manual of Patent Examining Procedure at § 2112. "The fact that a certain result or characteristic **may** occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *See id. citing In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The Applicants respectfully submit that neither Boucher itself nor the Office Action "make[s] clear that the missing descriptive matter," said to be inherent, i.e., that "it is inherent that **any packet** received would be inserted in its **correct placement** in host memory as shown by Figure 2," is "**necessarily present** in" Boucher.

A rejection based on inherency must be based on factual or technical reasoning:

> In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teaching of the applied prior art.

Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

The Applicants respectfully submit that the Office Action does not contain a basis in fact and/or technical reasoning to support the rejection based on inherency. Instead, as recited above, at least claim 9 of the present application stands rejected based on a conclusory statement of inherency, rather than upon a "basis in fact and/or technical reasoning." Accordingly, the Applicants respectfully maintain that, absent a "basis in fact and/or technical reasoning" that "it is inherent that **any packet** received would be inserted in its **correct placement** in host memory as shown by Figure 2" with respect to the rejection of claim 9, that rejection should be reconsidered and withdrawn.

III. Boucher Does Not Render Claim 6 Unpatentable

Claim 6 stands rejected as being unpatentable over Boucher. Initially, the Applicants respectfully submit that claim 6 should be in condition for allowance, at least for the reasons set forth above. The previous Office Action states the following:

> Boucher does not specifically state that only the elastic buffer is used to temporarily buffer at least a portion of the incoming TCP packet, however, it is well known that elastic buffers are used to buffer packets (i.e., receiving FIFO's for routers, etc.). By this rationale, **"Official Notice"** is taken that both the concept and advantages of providing for utilizing only the elastic buffer to temporarily buffer a portion of the TCP packet is well known and expected in the art.

See August 19, 2005 Office Action at page 6 (emphasis added). Further, the present Office Action maintains that "Boucher does not specifically state that

only the elastic buffer is used to temporarily buffer at least a portion of the incoming TCP packet." *See* October 7, 2005 Office Action at pages 4-5.

The Applicants traversed the clear assertion of Official Notice that "both the concept and advantages of providing for utilizing only the elastic buffer to temporarily buffer a portion of the TCP packet is well known and expected in the art." *See,* September 15, 2005 Amendment at pages 16-18. In response, the present Office Action states the following:

> [T]he Office provides Susnow et al (USPN 6,751,235) as support that only the elastic buffer is used to temporarily buffer at least a portion of the incoming packet. As shown in Figure 8, and col., 7, lines 30-55. It can clearly be seen that the elastic buffer is used to transition data from a network link to the core clock domain of the VXB (i.e. virtual expansion bridge) thereby removing the chance of providing data overflow or underflow. By this rationale, the Office has satisfied its burden of proof that an elastic buffer can be used to buffer a portion of an incoming packet is well known in the art.

See October 7, 2005 Office Action at pages 6-7. In short, the present Office Action asserts that it has satisfied it burden of proof "that an elastic buffer can be used to buffer a portion of an incoming packet."

The Office Action, however, rejects claim 6 of the present application through an assertion of Official Notice. Claim 6 recites the following:

> The system according to claim 1, wherein said NIC utilizes **only said at least one internal elastic buffer** to temporarily buffer said at least a portion of said incoming TCP packet.

The Applicants are not disputing that elastic buffers exist. Further, United States Patent No. 6,751,235 ("Susnow") does, indeed, disclose an elastic buffer. *See*

Susnow at column 7, lines 35-39 ("FIG. 8 illustrates an example block diagram of Elastic Buffer 682 provided to transition data from a network link into the core clock domain of VXB 670 responsible for transferring that data to MCH 620 without data overflow or data underflow....").

Claim 6, however, recites that "**only** said at least one **internal** elastic buffer [is utilized] to temporarily buffer said at least a portion of said incoming TCP packet." Further, even assuming the Office Action has "satisfied its burden of proof that an elastic buffer can be used to buffer a portion of an incoming packet," the Office Action still does not show a reference in which "**only** said at least one internal elastic buffer is utilized to temporarily buffer said at least a portion of said incoming TCP packet." Thus, the Applicants reaffirm the traversal of Official Notice. Under MPEP 2144.03, the Examiner continues to be obligated to provide a reference(s) in support of the assertion of Official Notice with respect to claim 6 (i.e., "only said at least one internal elastic buffer [is utilized] to temporarily buffer said at least a portion of said incoming TCP packet") if the Examiner intends to maintain any rejection based on the assertion of Official Notice. Additionally, the Applicants respectfully request the Examiner reconsider the assertion of Official Notice and provide to Applicants any basis for the assertion of Official Notice.

IV. Conclusion

The Applicants respectfully submit that the claims of the present application should be in condition for allowance at least for the reasons discussed above and requests that the outstanding rejections be reconsidered

and withdrawn. If the Examiner has any questions or the Applicants can be of any assistance, the Examiner is invited to contact the Applicants. The Commissioner is authorized to charge any necessary fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

Date: November 22, 2005

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